

Charge Pump DC-to-DC Voltage Converter

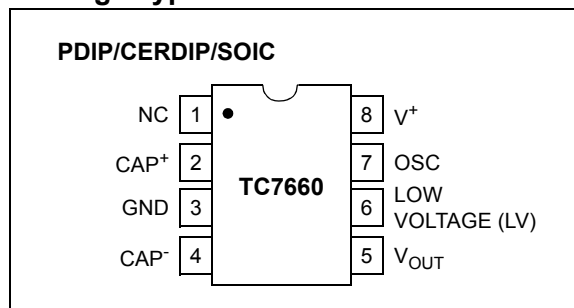
Features

- Wide Input Voltage Range: +1.5V to +10V
- Efficient Voltage Conversion (99.9%, typ)
- Excellent Power Efficiency (98%, typ)
- Low Power Consumption: 80 μ A (typ) @ $V_{IN} = 5V$
- Low Cost and Easy to Use
 - Only Two External Capacitors Required
- Available in 8-Pin Small Outline (SOIC), 8-Pin PDIP and 8-Pin Cerdip Packages
- Improved ESD Protection (3 kV HBM)
- No External Diode Required for High-Voltage Operation

Applications

- RS-232 Negative Power Supply
- Simple Conversion of +5V to $\pm 5V$ Supplies
- Voltage Multiplication $V_{OUT} = \pm n V^+$
- Negative Supplies for Data Acquisition Systems and Instrumentation

Package Types



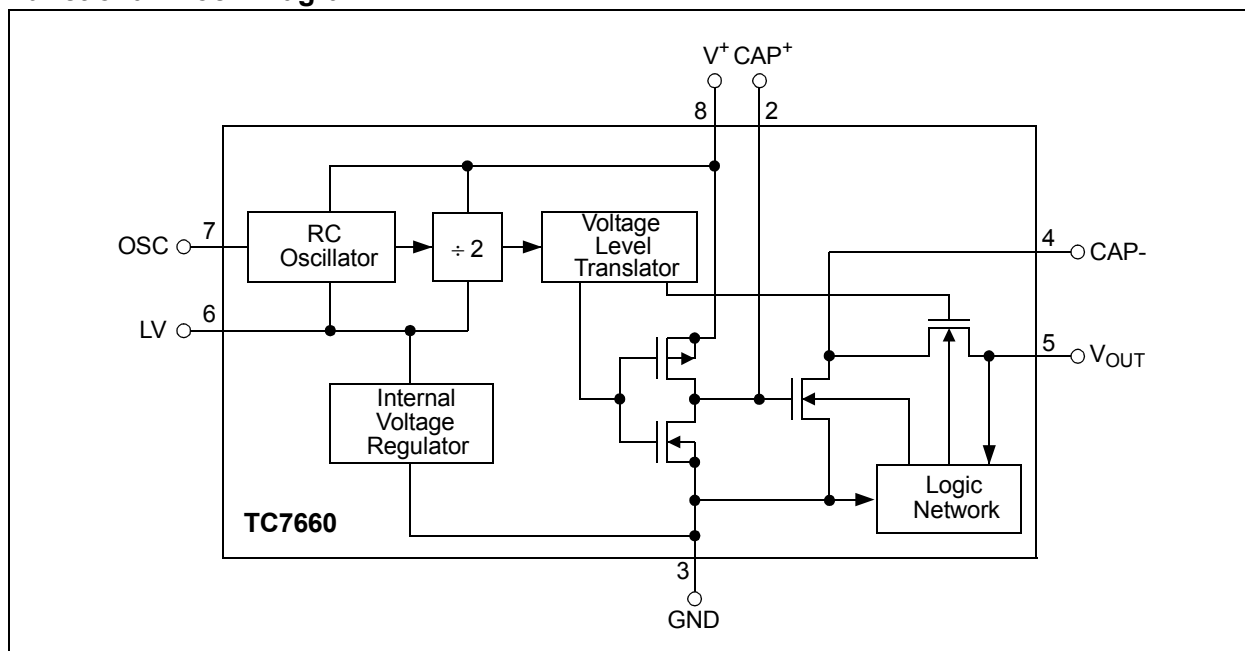
General Description

The TC7660 device is a pin-compatible replacement for the industry standard 7660 charge pump voltage converter. It converts a +1.5V to +10V input to a corresponding -1.5V to -10V output using only two low-cost capacitors, eliminating inductors and their associated cost, size and electromagnetic interference (EMI).

The on-board oscillator operates at a nominal frequency of 10 kHz. Operation below 10 kHz (for lower supply current applications) is possible by connecting an external capacitor from OSC to ground.

The TC7660 is available in 8-Pin PDIP, 8-Pin Small Outline (SOIC) and 8-Pin Cerdip packages in commercial and extended temperature ranges.

Functional Block Diagram



TC7660

1.0 ELECTRICAL CHARACTERISTICS

Absolute Maximum Ratings*

Supply Voltage	+10.5V
LV and OSC Inputs Voltage: (Note 1)	
.....	-0.3V to V_{SS} for $V^+ < 5.5V$
.....	$(V^+ - 5.5V)$ to (V^+) for $V^+ > 5.5V$
Current into LV	20 μA for $V^+ > 3.5V$
Output Short Duration ($V_{SUPPLY} \leq 5.5V$).....	Continuous
Package Power Dissipation: ($T_A \leq 70^\circ C$)	
8-Pin CERDIP	800 mW
8-Pin PDIP	730 mW
8-Pin SOIC	470 mW
Operating Temperature Range:	
C Suffix	0°C to +70°C
I Suffix	-25°C to +85°C
E Suffix	-40°C to +85°C
M Suffix	-55°C to +125°C
Storage Temperature Range	-65°C to +160°C
ESD protection on all pins (HBM)	≥ 3 kV
Maximum Junction Temperature	150°C

* **Notice:** Stresses above those listed under “Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operational sections of this specification is not intended. Exposure to maximum rating conditions for extended periods may affect device reliability.

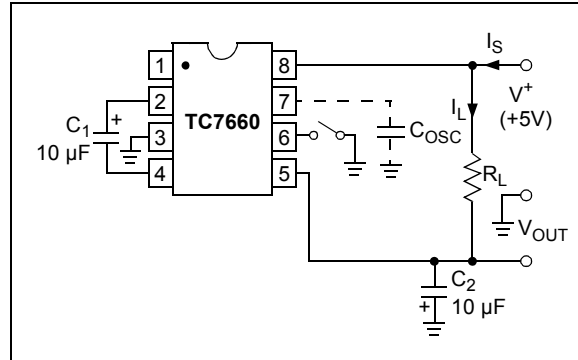


FIGURE 1-1: TC7660 Test Circuit.

ELECTRICAL SPECIFICATIONS

Electrical Characteristics: Unless otherwise noted, specifications measured over operating temperature range with $V^+ = 5V$, $C_{OSC} = 0$, refer to test circuit in Figure 1-1.

Parameters	Sym	Min	Typ	Max	Units	Conditions
Supply Current	I^+	—	80	180	μA	$R_L = \infty$
Supply Voltage Range, High	V^+_H	3.0	—	10	V	$Min \leq T_A \leq Max$, $R_L = 10$ k Ω , LV Open
Supply Voltage Range, Low	V^+_L	1.5	—	3.5	V	$Min \leq T_A \leq Max$, $R_L = 10$ k Ω , LV to GND
Output Source Resistance	R_{OUT}	—	70	100	Ω	$I_{OUT} = 20$ mA, $T_A = +25^\circ C$
		—	—	120		$I_{OUT} = 20$ mA, $T_A \leq +70^\circ C$ (C Device)
		—	—	130		$I_{OUT} = 20$ mA, $T_A \leq +85^\circ C$ (E and I Device)
		—	104	150		$I_{OUT} = 20$ mA, $T_A \leq +125^\circ C$ (M Device)
		—	150	300		$V^+ = 2V$, $I_{OUT} = 3$ mA, LV to GND $0^\circ C \leq T_A \leq +70^\circ C$
		—	160	600		$V^+ = 2V$, $I_{OUT} = 3$ mA, LV to GND $-55^\circ C \leq T_A \leq +125^\circ C$ (M Device)
Oscillator Frequency	f_{OSC}	—	10	—	kHz	Pin 7 open
Power Efficiency	P_{EFF}	95	98	—	%	$R_L = 5$ k Ω
Voltage Conversion Efficiency	V_{OUTEFF}	97	99.9	—	%	$R_L = \infty$
Oscillator Impedance	Z_{OSC}	—	1.0	—	M Ω	$V^+ = 2V$
		—	100	—	k Ω	$V^+ = 5V$

Note 1: Destructive latch-up may occur if voltages greater than V^+ or less than GND are supplied to any input pin.

2.0 TYPICAL PERFORMANCE CURVES

Note: The graphs and tables provided following this note are a statistical summary based on a limited number of samples and are provided for informational purposes only. The performance characteristics listed herein are not tested or guaranteed. In some graphs or tables, the data presented may be outside the specified operating range (e.g., outside specified power supply range) and therefore outside the warranted range.

Note: Unless otherwise indicated, $C_1 = C_2 = 10 \mu\text{F}$, $\text{ESR}_{C1} = \text{ESR}_{C2} = 1 \Omega$, $T_A = 25^\circ\text{C}$. See Figure 1-1.

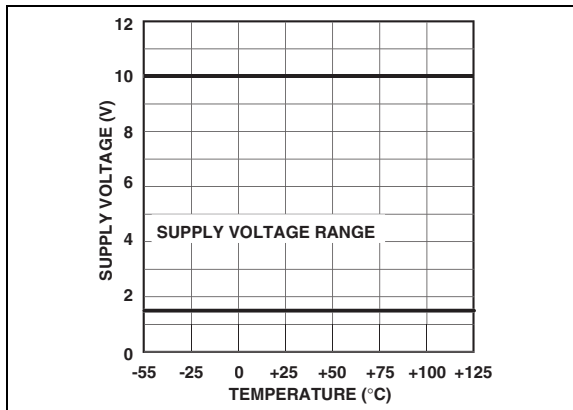


FIGURE 2-1: Operating Voltage vs. Temperature.

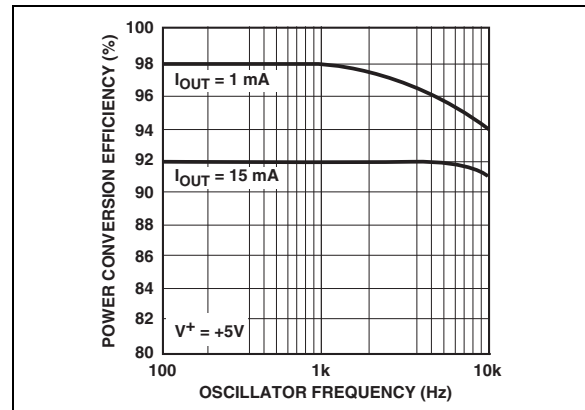


FIGURE 2-4: Power Conversion Efficiency vs. Oscillator Frequency.

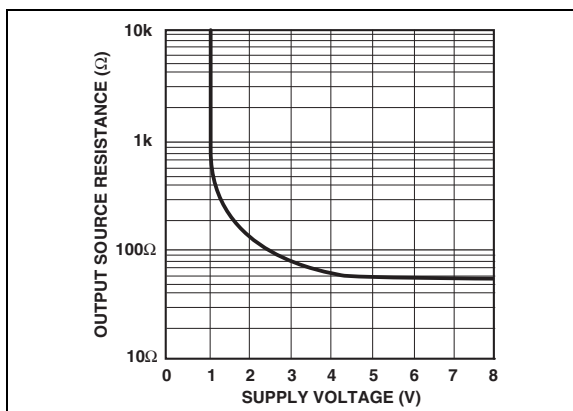


FIGURE 2-2: Output Source Resistance vs. Supply Voltage.

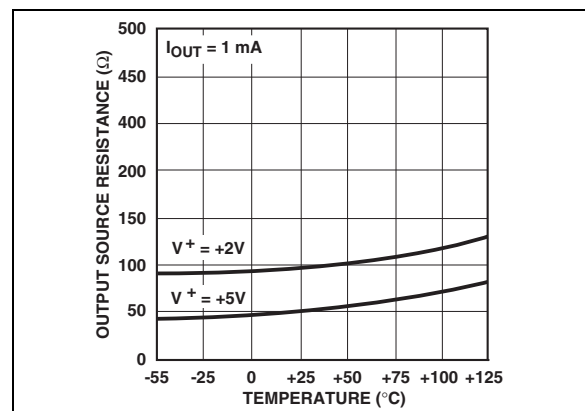


FIGURE 2-5: Output Source Resistance vs. Temperature.

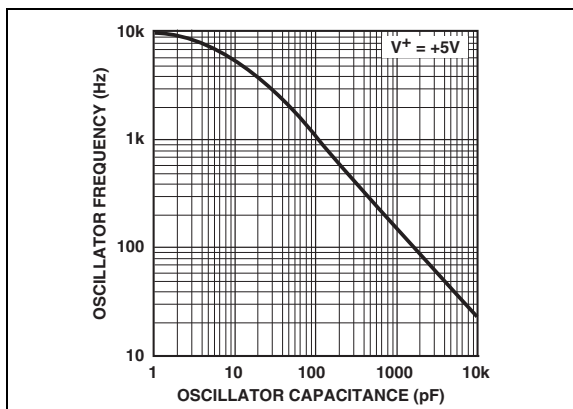


FIGURE 2-3: Frequency of Oscillation vs. Oscillator Capacitance.

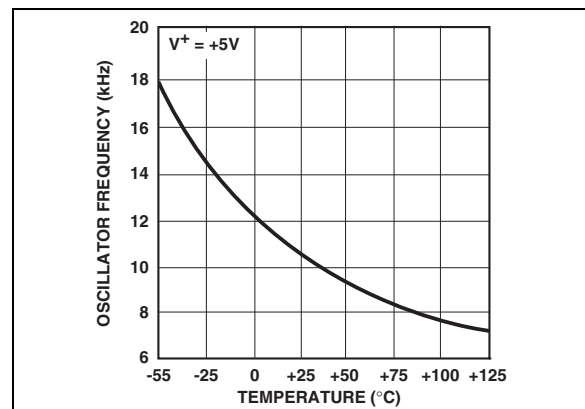


FIGURE 2-6: Unloaded Oscillator Frequency vs. Temperature.

TC7660

Note: Unless otherwise indicated, $C_1 = C_2 = 10 \mu\text{F}$, $\text{ESR}_{C1} = \text{ESR}_{C2} = 1 \Omega$, $T_A = 25^\circ\text{C}$. See Figure 1-1.

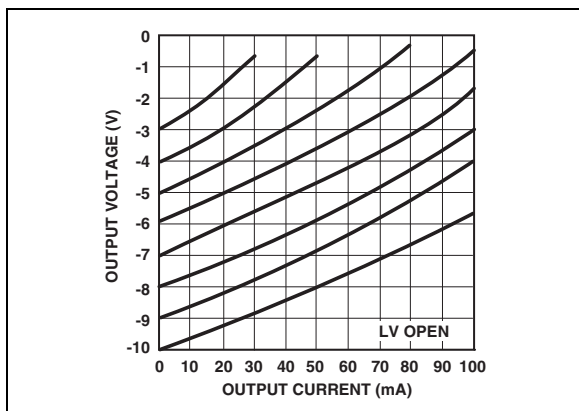


FIGURE 2-7: Output Voltage vs. Output Current.

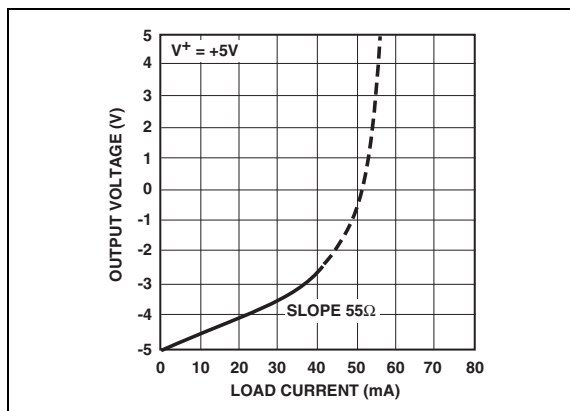


FIGURE 2-10: Output Voltage vs. Load Current.

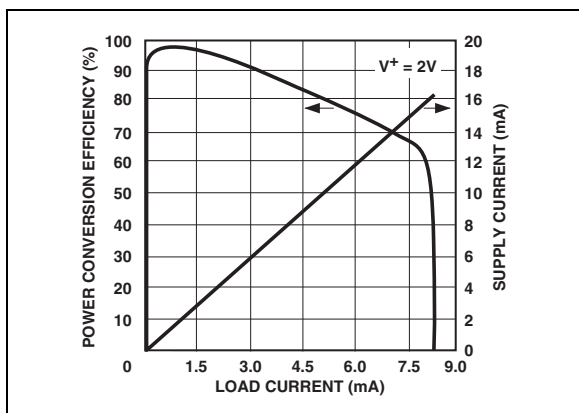


FIGURE 2-8: Supply Current and Power Conversion Efficiency vs. Load Current.

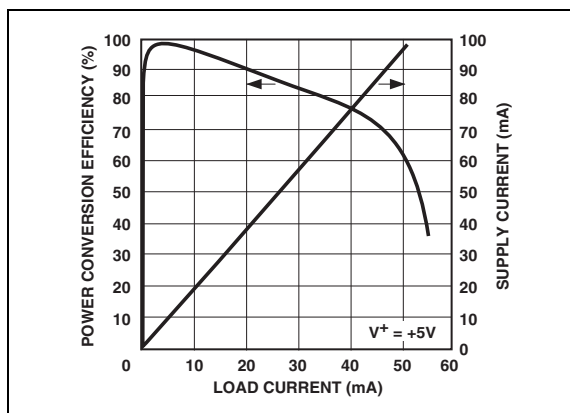


FIGURE 2-11: Supply Current and Power Conversion Efficiency vs. Load Current.

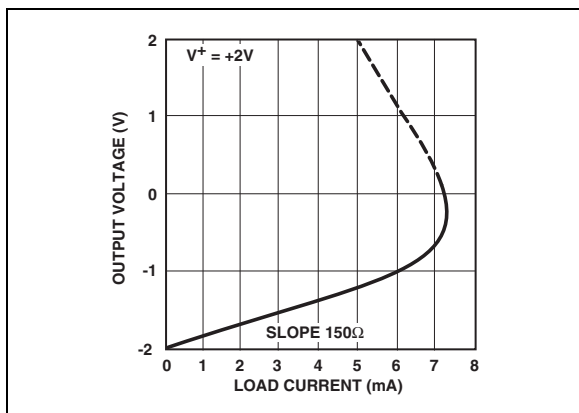


FIGURE 2-9: Output Voltage vs. Load Current.

3.0 PIN DESCRIPTIONS

The descriptions of the pins are listed in [Table 3-1](#).

TABLE 3-1: PIN FUNCTION TABLE

Pin No.	Symbol	Description
1	NC	No connection
2	CAP ⁺	Charge pump capacitor positive terminal
3	GND	Ground terminal
4	CAP ⁻	Charge pump capacitor negative terminal
5	V _{OUT}	Output voltage
6	LV	Low voltage pin. Connect to GND for V ₊ < 3.5V
7	OSC	Oscillator control input. Bypass with an external capacitor to slow the oscillator
8	V ⁺	Power supply positive voltage input

3.1 Charge Pump Capacitor (CAP⁺)

Positive connection for the charge pump capacitor, or flying capacitor, used to transfer charge from the input source to the output. In the voltage-inverting configuration, the charge pump capacitor is charged to the input voltage during the first half of the switching cycle. During the second half of the switching cycle, the charge pump capacitor is inverted and charge is transferred to the output capacitor and load.

It is recommended that a low ESR (equivalent series resistance) capacitor be used. Additionally, larger values will lower the output resistance.

3.2 Ground (GND)

Input and output zero volt reference.

3.3 Charge Pump Capacitor (CAP⁻)

Negative connection for the charge pump capacitor, or flying capacitor, used to transfer charge from the input to the output. Proper orientation is imperative when using a polarized capacitor.

3.4 Output Voltage (V_{OUT})

Negative connection for the charge pump output capacitor. In the voltage-inverting configuration, the charge pump output capacitor supplies the output load during the first half of the switching cycle. During the second half of the switching cycle, charge is restored to the charge pump output capacitor.

It is recommended that a low ESR (equivalent series resistance) capacitor be used. Additionally, larger values will lower the output ripple.

3.5 Low Voltage Pin (LV)

The low voltage pin ensures proper operation of the internal oscillator for input voltages below 3.5V. The low voltage pin should be connected to ground (GND) for input voltages below 3.5V. Otherwise, the low voltage pin should be allowed to float.

3.6 Oscillator Control Input (OSC)

The oscillator control input can be utilized to slow down or speed up the operation of the TC7660. Refer to [Section 5.4 “Changing the TC7660 Oscillator Frequency”](#), for details on altering the oscillator frequency.

3.7 Power Supply (V⁺)

Positive power supply input voltage connection. It is recommended that a low ESR (equivalent series resistance) capacitor be used to bypass the power supply input to ground (GND).

4.0 DETAILED DESCRIPTION

4.1 Theory of Operation

The TC7660 charge pump converter inverts the voltage applied to the V^+ pin. The conversion consists of a two-phase operation (Figure 4-1). During the first phase, switches S_2 and S_4 are open and switches S_1 and S_3 are closed. C_1 charges to the voltage applied to the V^+ pin, with the load current being supplied from C_2 . During the second phase, switches S_2 and S_4 are closed and switches S_1 and S_3 are open. Charge is transferred from C_1 to C_2 , with the load current being supplied from C_1 .

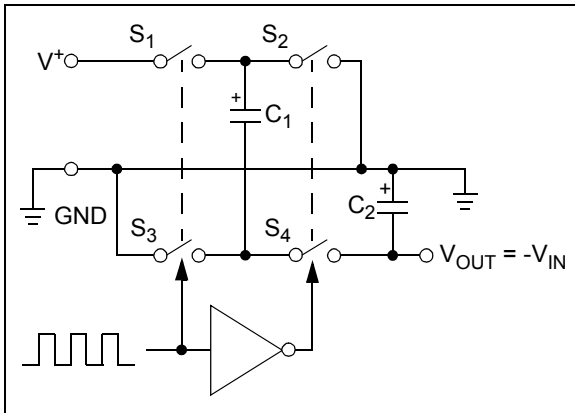


FIGURE 4-1: Ideal Switched Capacitor Inverter.

In this manner, the TC7660 performs a voltage inversion, but does not provide regulation. The average output voltage will drop in a linear manner with respect to load current. The equivalent circuit of the charge pump inverter can be modeled as an ideal voltage source in series with a resistor, as shown in Figure 4-2.

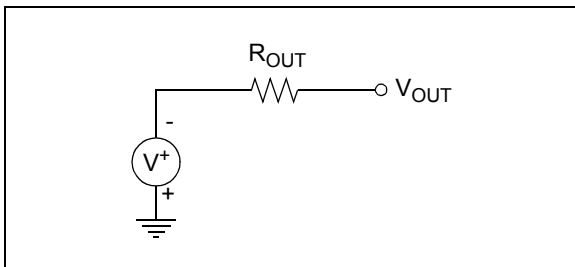


FIGURE 4-2: Switched Capacitor Inverter Equivalent Circuit Model.

The value of the series resistor (R_{OUT}) is a function of the switching frequency, capacitance and equivalent series resistance (ESR) of C_1 and C_2 and the on-resistance of switches S_1 , S_2 , S_3 and S_4 . A close approximation for R_{OUT} is given in the following equation:

EQUATION

$$R_{OUT} = \left[\frac{1}{f_{PUMP} \times C_1} + 8R_{SW} + 4ESR_{C1} + ESR_{C2} \right]$$

Where:

$$f_{PUMP} = \frac{f_{OSC}}{2}$$

R_{SW} = on-resistance of the switches

ESR_{C1} = equivalent series resistance of C_1

ESR_{C2} = equivalent series resistance of C_2

4.2 Switched Capacitor Inverter Power Losses

The overall power loss of a switched capacitor inverter is affected by four factors:

1. Losses from power consumed by the internal oscillator, switch drive, etc. These losses will vary with input voltage, temperature and oscillator frequency.
2. Conduction losses in the non-ideal switches.
3. Losses due to the non-ideal nature of the external capacitors.
4. Losses that occur during charge transfer from C_1 to C_2 when a voltage difference between the capacitors exists.

Figure 4-3 depicts the non-ideal elements associated with the switched capacitor inverter power loss.

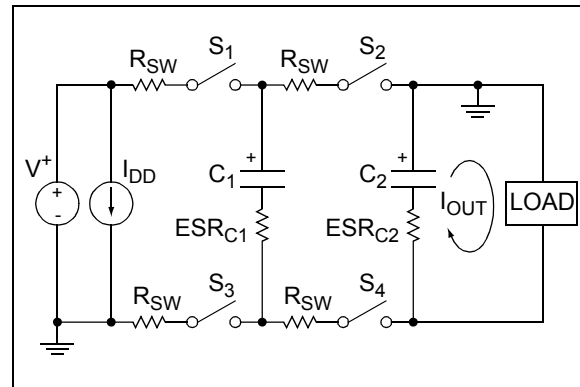


FIGURE 4-3: Non-Ideal Switched Capacitor Inverter.

The power loss is calculated using the following equation:

EQUATION

$$P_{LOSS} = I_{OUT}^2 \times R_{OUT} + I_{DD} \times V^+$$

5.0 APPLICATIONS INFORMATION

5.1 Simple Negative Voltage Converter

Figure 5-1 shows typical connections to provide a negative supply where a positive supply is available. A similar scheme may be employed for supply voltages anywhere in the operating range of +1.5V to +10V, keeping in mind that pin 6 (LV) is tied to the supply negative (GND) only for supply voltages below 3.5V.

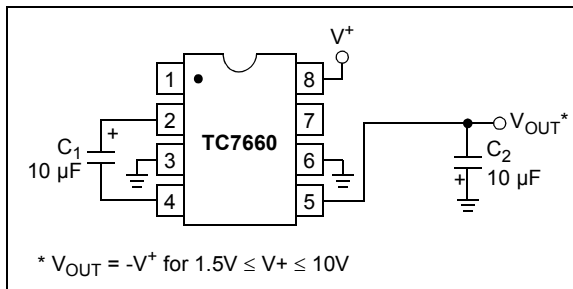


FIGURE 5-1: Simple Negative Converter.

The output characteristics of the circuit in Figure 5-1 are those of a nearly ideal voltage source in series with a 70Ω resistor. Thus, for a load current of -10 mA and a supply voltage of +5V, the output voltage would be -4.3V.

5.2 Paralleling Devices

To reduce the value of R_{OUT} , multiple TC7660 voltage converters can be connected in parallel (Figure 5-2). The output resistance will be reduced by approximately a factor of n , where n is the number of devices connected in parallel.

EQUATION

$$R_{OUT} = \frac{R_{OUT}(\text{of TC7660})}{n(\text{number of devices})}$$

While each device requires its own pump capacitor (C_1), all devices may share one reservoir capacitor (C_2). To preserve ripple performance, the value of C_2 should be scaled according to the number of devices connected in parallel.

5.3 Cascading Devices

A larger negative multiplication of the initial supply voltage can be obtained by cascading multiple TC7660 devices. The output voltage and the output resistance will both increase by approximately a factor of n , where n is the number of devices cascaded.

EQUATION

$$V_{OUT} = -n(V^+)$$

$$R_{OUT} = n \times R_{OUT}(\text{of TC7660})$$

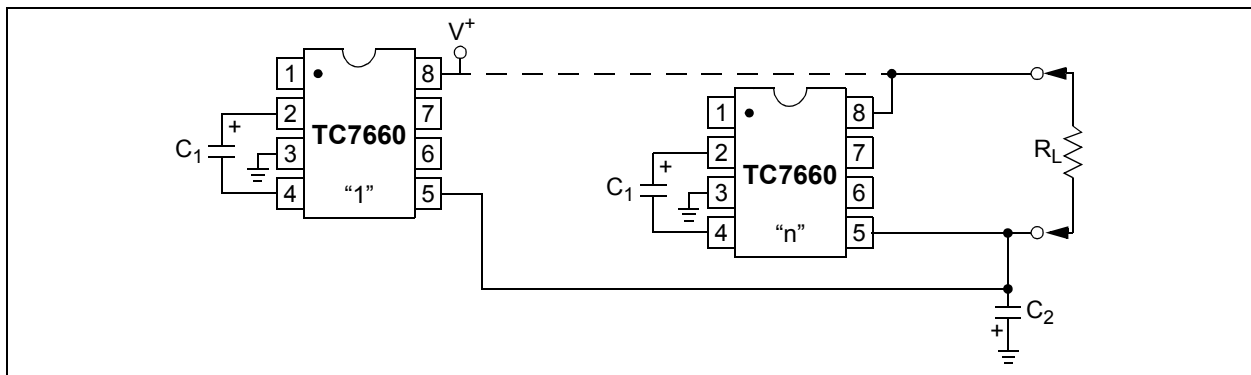


FIGURE 5-2: Paralleling Devices Lowers Output Impedance.

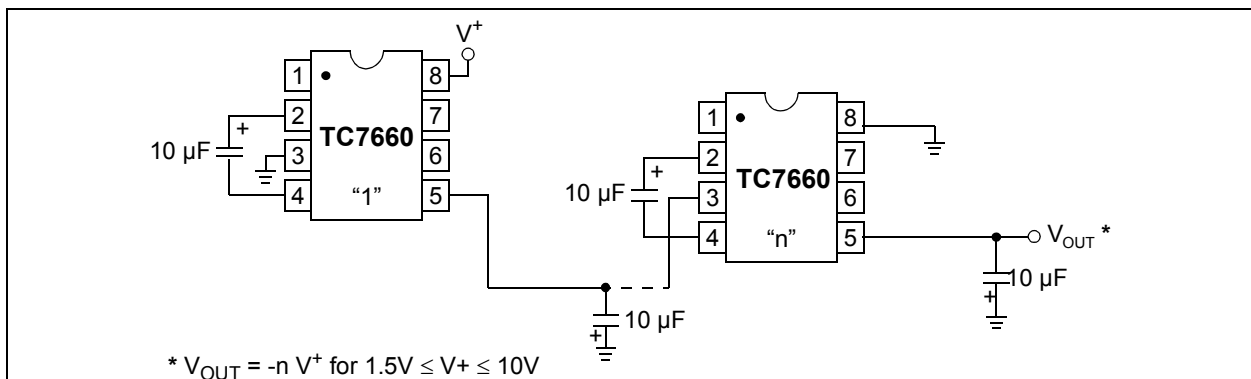


FIGURE 5-3: Increased Output Voltage By Cascading Devices.

TC7660

5.4 Changing the TC7660 Oscillator Frequency

The operating frequency of the TC7660 can be changed in order to optimize the system performance. The frequency can be increased by over-driving the OSC input (Figure 5-4). Any CMOS logic gate can be utilized in conjunction with a 1 kΩ series resistor. The resistor is required to prevent device latch-up. While TTL level signals can be utilized, an additional 10 kΩ pull-up resistor to V⁺ is required. Transitions occur on the rising edge of the clock input. The resultant output voltage ripple frequency is one half the clock input. Higher clock frequencies allow for the use of smaller pump and reservoir capacitors for a given output voltage ripple and droop. Additionally, this allows the TC7660 to be synchronized to an external clock, eliminating undesirable beat frequencies.

At light loads, lowering the oscillator frequency can increase the efficiency of the TC7660 (Figure 5-5). By lowering the oscillator frequency, the switching losses are reduced. Refer to Figure 2-3 to determine the typical operating frequency based on the value of the external capacitor. At lower operating frequencies, it may be necessary to increase the values of the pump and reservoir capacitors in order to maintain the desired output voltage ripple and output impedance.

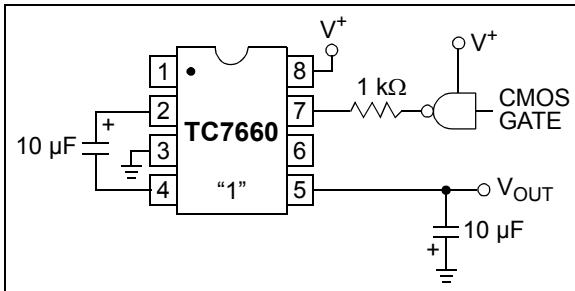


FIGURE 5-4: External Clocking.

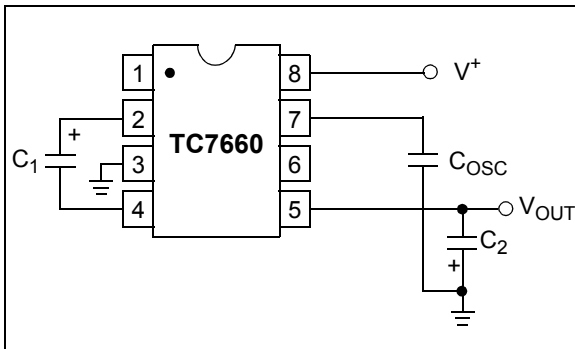


FIGURE 5-5: Lowering Oscillator Frequency.

5.5 Positive Voltage Multiplication

Positive voltage multiplication can be obtained by employing two external diodes (Figure 5-6). Refer to the theory of operation of the TC7660 (Section 4.1 “Theory of Operation”). During the half cycle when switch S₂ is closed, capacitor C₁ of Figure 5-6 is charged up to a voltage of V⁺ - V_{F1}, where V_{F1} is the forward voltage drop of diode D₁. During the next half cycle, switch S₁ is closed, shifting the reference of capacitor C₁ from GND to V⁺. The energy in capacitor C₁ is transferred to capacitor C₂ through diode D₂, producing an output voltage of approximately:

EQUATION

$$V_{OUT} = 2 \times V^+ - (V_{F1} + V_{F2})$$

where:

V_{F1} is the forward voltage drop of diode D₁
and
V_{F2} is the forward voltage drop of diode D₂.

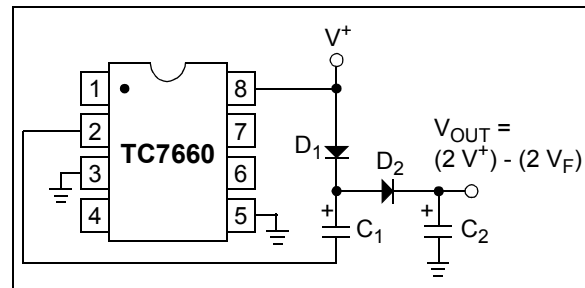


FIGURE 5-6: Positive Voltage Multiplier.

5.6 Combined Negative Voltage Conversion and Positive Supply Multiplication

Simultaneous voltage inversion and positive voltage multiplication can be obtained (Figure 5-7). Capacitors C₁ and C₃ perform the voltage inversion, while capacitors C₂ and C₄, plus the two diodes, perform the positive voltage multiplication. Capacitors C₁ and C₂ are the pump capacitors, while capacitors C₃ and C₄ are the reservoir capacitors for their respective functions. Both functions utilize the same switches of the TC7660. As a result, if either output is loaded, both outputs will drop towards GND.

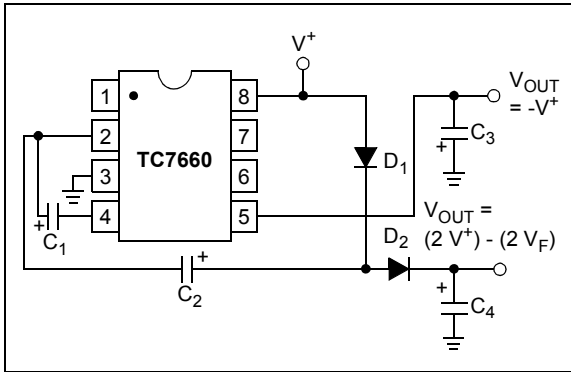


FIGURE 5-7: Combined Negative Converter and Positive Multiplier.

5.7 Efficient Positive Voltage Multiplication/Conversion

Since the switches that allow the charge pumping operation are bidirectional, the charge transfer can be performed backwards as easily as forwards. [Figure 5-8](#) shows a TC7660 transforming $-5V$ to $+5V$ (or $+5V$ to $+10V$, etc.). The only problem here is that the internal clock and switch-drive section will not operate until some positive voltage has been generated. An initial inefficient pump, as shown in [Figure 5-7](#), could be used to start this circuit up, after which it will bypass the other (D_1 and D_2 in [Figure 5-7](#) would never turn on), or else the diode and resistor shown dotted in [Figure 5-8](#) can be used to “force” the internal regulator on.

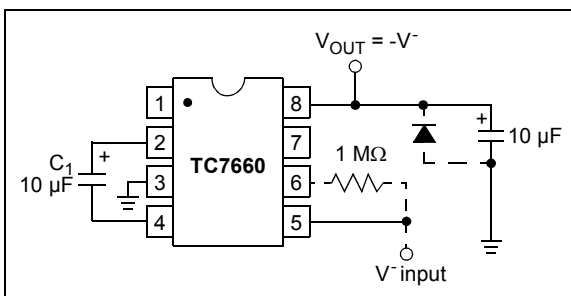


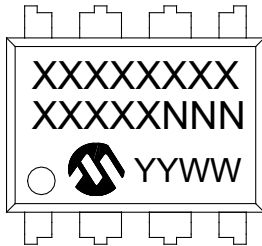
FIGURE 5-8: Positive Voltage Conversion.

TC7660

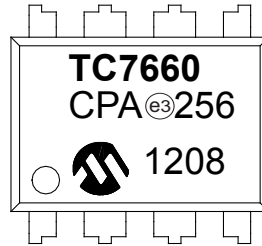
6.0 PACKAGING INFORMATION

6.1 Package Marking Information

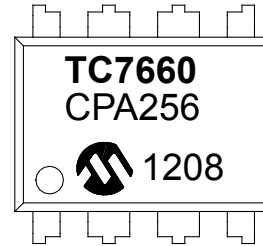
8-Lead PDIP (300 mil)



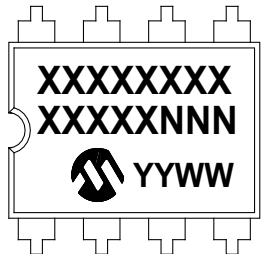
Example



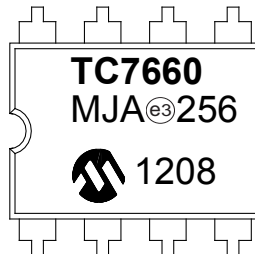
Example



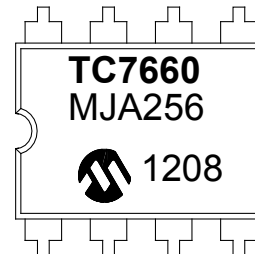
8-Lead CERDIP (.300")



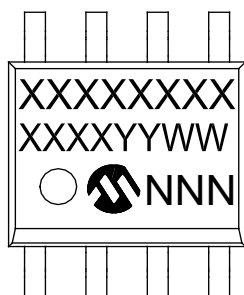
Example



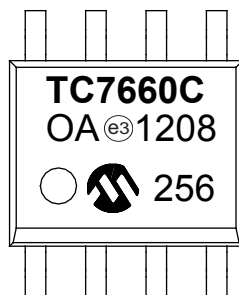
Example



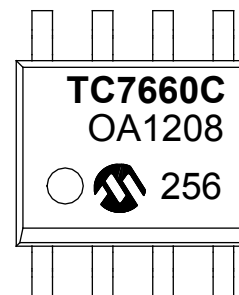
8-Lead SOIC (3.90 mm)



Example



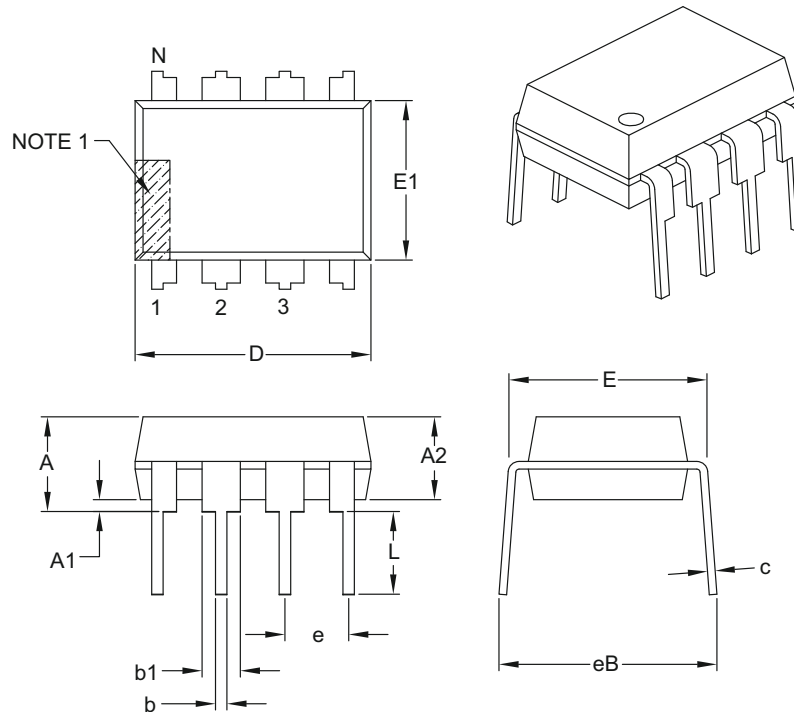
Example



Legend:	XX...X	Customer-specific information
	Y	Year code (last digit of calendar year)
	YY	Year code (last 2 digits of calendar year)
	WW	Week code (week of January 1 is week '01')
	NNN	Alphanumeric traceability code
	^{e3}	Pb-free JEDEC designator for Matte Tin (Sn)
	*	This package is Pb-free. The Pb-free JEDEC designator (^{e3}) can be found on the outer packaging for this package.
Note:	In the event the full Microchip part number cannot be marked on one line, it will be carried over to the next line thus limiting the number of available characters for customer specific information.	

8-Lead Plastic Dual In-Line (PA) – 300 mil Body [PDIP]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at <http://www.microchip.com/packaging>



Dimension Limits	Units	INCHES		
		MIN	NOM	MAX
Number of Pins	N	8		
Pitch	e	.100 BSC		
Top to Seating Plane	A	–	–	.210
Molded Package Thickness	A2	.115	.130	.195
Base to Seating Plane	A1	.015	–	–
Shoulder to Shoulder Width	E	.290	.310	.325
Molded Package Width	E1	.240	.250	.280
Overall Length	D	.348	.365	.400
Tip to Seating Plane	L	.115	.130	.150
Lead Thickness	c	.008	.010	.015
Upper Lead Width	b1	.040	.060	.070
Lower Lead Width	b	.014	.018	.022
Overall Row Spacing §	eB	–	–	.430

Notes:

- Pin 1 visual index feature may vary, but must be located with the hatched area.
- § Significant Characteristic.
- Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed .010" per side.
- Dimensioning and tolerancing per ASME Y14.5M.

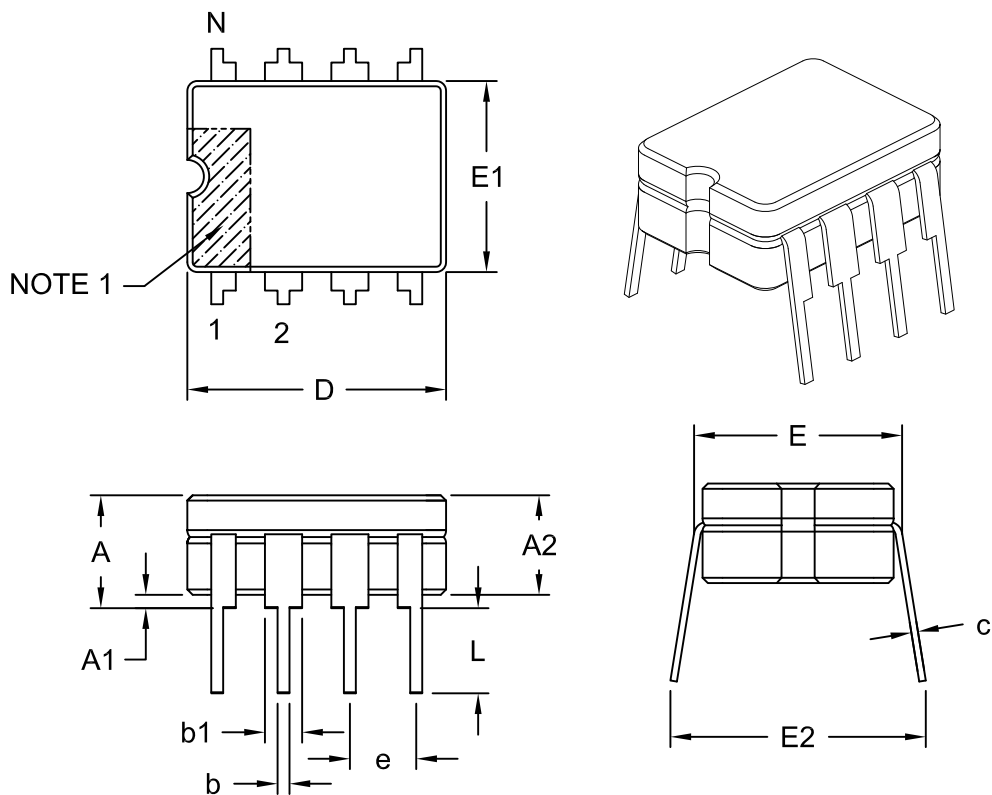
BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing C04-018B

TC7660

8-Lead Ceramic Dual In-Line (JA) ~ .300" Body [CERDIP]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at <http://www.microchip.com/packaging>



Dimension Limits	Units	INCHES		
		MIN	NOM	MAX
Number of Pins	N	8		
Pitch	e	.100 BSC		
Top to Seating Plane	A	-	-	.200
Base to Seating Plane §	A1	.015	-	-
Ceramic Package Height	A2	.140	-	.175
Shoulder to Shoulder Width	E	.290	-	.320
Ceramic Pkg. Width	E1	.230	.248	.300
Overall Length	D	.370	.380	.400
Tip to Seating Plane	L	.125	-	.200
Lead Thickness	c	.008	-	.015
Upper Lead Width	b1	.045	-	.065
Lower Lead Width	b	.015	-	.023
Overall Row Spacing	E2	.314	-	.410

Notes:

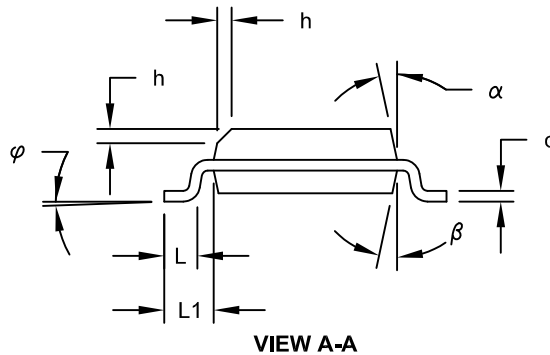
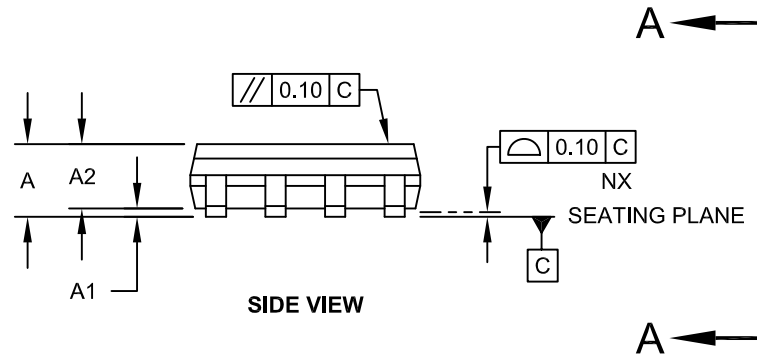
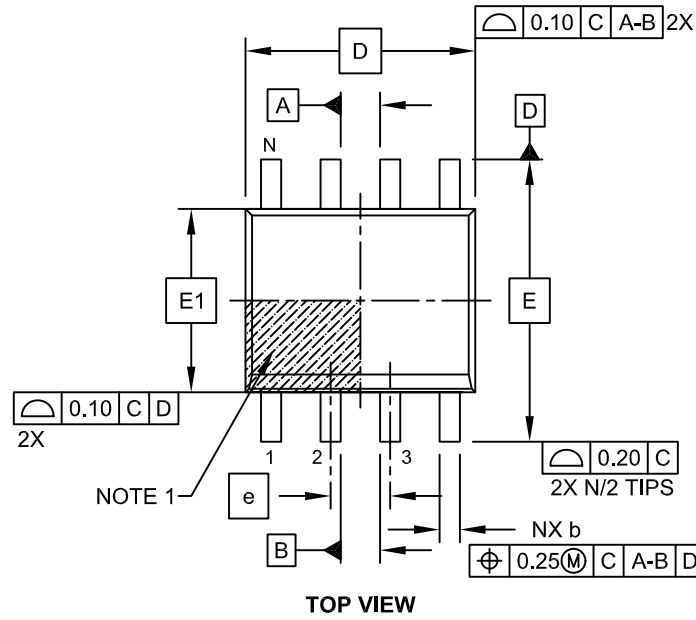
- Pin 1 visual index feature may vary, but must be located within the hatched area.
- § Significant Characteristic
- Dimensioning and tolerancing per ASME Y14.5M

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing No. C04-001C

8-Lead Plastic Small Outline (OA) - Narrow, 3.90 mm Body [SOIC]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at <http://www.microchip.com/packaging>

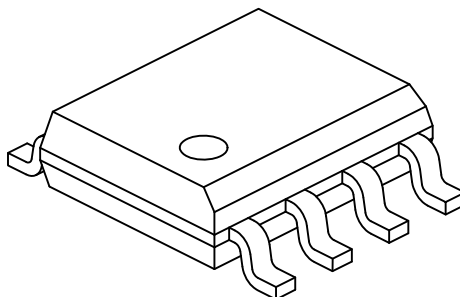


Microchip Technology Drawing No. C04-057C Sheet 1 of 2

TC7660

8-Lead Plastic Small Outline (OA) - Narrow, 3.90 mm Body [SOIC]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at <http://www.microchip.com/packaging>



Dimension Limits	Units	MILLIMETERS		
		MIN	NOM	MAX
Number of Pins	N	8		
Pitch	e	1.27 BSC		
Overall Height	A	-	-	1.75
Molded Package Thickness	A2	1.25	-	-
Standoff §	A1	0.10	-	0.25
Overall Width	E	6.00 BSC		
Molded Package Width	E1	3.90 BSC		
Overall Length	D	4.90 BSC		
Chamfer (Optional)	h	0.25	-	0.50
Foot Length	L	0.40	-	1.27
Footprint	L1	1.04 REF		
Foot Angle	φ	0°	-	8°
Lead Thickness	c	0.17	-	0.25
Lead Width	b	0.31	-	0.51
Mold Draft Angle Top	α	5°	-	15°
Mold Draft Angle Bottom	β	5°	-	15°

Notes:

1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. § Significant Characteristic
3. Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.15mm per side.
4. Dimensioning and tolerancing per ASME Y14.5M

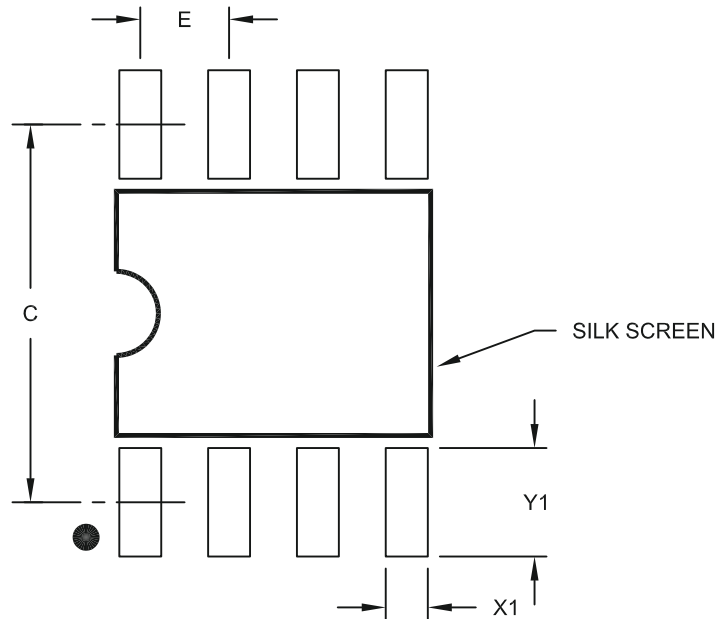
BSC: Basic Dimension. Theoretically exact value shown without tolerances.

REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing No. C04-057C Sheet 2 of 2

8-Lead Plastic Small Outline (OA) – Narrow, 3.90 mm Body [SOIC]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at <http://www.microchip.com/packaging>



RECOMMENDED LAND PATTERN

Dimension Limits	Units	MILLIMETERS		
		MIN	NOM	MAX
Contact Pitch	E	1.27 BSC		
Contact Pad Spacing	C		5.40	
Contact Pad Width (X8)	X1			0.60
Contact Pad Length (X8)	Y1			1.55

Notes:

1. Dimensioning and tolerancing per ASME Y14.5M

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing No. C04-2057A

APPENDIX A: REVISION HISTORY

Revision C (March 2012)

The following is the list of modifications.

1. Updated [Figure 5-5](#).
2. Added Appendix A.

Revision B (March 2003)

Undocumented changes.

Revision A (May 2002)

Original release of this document.

PRODUCT IDENTIFICATION SYSTEM

To order or obtain information, e.g., on pricing or delivery, refer to the factory or the listed sales office.

<u>PART NO.</u>		<u>X</u>	<u>/XX</u>
Device	Temperature Range		Package
Device:	TC7660:		DC-to-DC Voltage Converter
Temperature Range:	C =		0°C to +70°C
	E =		-40°C to +85°C
	I =		-25°C to +85°C (CERDIP only)
	M =		-55°C to +125°C (CERDIP only)
Package:	PA =		Plastic DIP, (300 mil body), 8-lead
	JA =		Ceramic DIP, (300 mil body), 8-lead
	OA =		SOIC (Narrow), 8-lead
	OA713 =		SOIC (Narrow), 8-lead (Tape and Reel)

Examples:

- a) TC7660COA: Commercial Temp., SOIC package.
- b) TC7660COA713: Tape and Reel, Commercial Temp., SOIC package.
- c) TC7660CPA: Commercial Temp., PDIP package.
- d) TC7660EOA: Extended Temp., SOIC package.
- e) TC7660EOA713: Tape and Reel, Extended Temp., SOIC package.
- f) TC7660EPA: Extended Temp., PDIP package.
- g) TC7660IJA: Industrial Temp., CERDIP package
- h) TC7660MJA: Military Temp., CERDIP package.

TC7660

NOTES:

Note the following details of the code protection feature on Microchip devices:

- Microchip products meet the specification contained in their particular Microchip Data Sheet.
- Microchip believes that its family of products is one of the most secure families of its kind on the market today, when used in the intended manner and under normal conditions.
- There are dishonest and possibly illegal methods used to breach the code protection feature. All of these methods, to our knowledge, require using the Microchip products in a manner outside the operating specifications contained in Microchip's Data Sheets. Most likely, the person doing so is engaged in theft of intellectual property.
- Microchip is willing to work with the customer who is concerned about the integrity of their code.
- Neither Microchip nor any other semiconductor manufacturer can guarantee the security of their code. Code protection does not mean that we are guaranteeing the product as “unbreakable.”

Code protection is constantly evolving. We at Microchip are committed to continuously improving the code protection features of our products. Attempts to break Microchip's code protection feature may be a violation of the Digital Millennium Copyright Act. If such acts allow unauthorized access to your software or other copyrighted work, you may have a right to sue for relief under that Act.

Information contained in this publication regarding device applications and the like is provided only for your convenience and may be superseded by updates. It is your responsibility to ensure that your application meets with your specifications. MICROCHIP MAKES NO REPRESENTATIONS OR WARRANTIES OF ANY KIND WHETHER EXPRESS OR IMPLIED, WRITTEN OR ORAL, STATUTORY OR OTHERWISE, RELATED TO THE INFORMATION, INCLUDING BUT NOT LIMITED TO ITS CONDITION, QUALITY, PERFORMANCE, MERCHANTABILITY OR FITNESS FOR PURPOSE. Microchip disclaims all liability arising from this information and its use. Use of Microchip devices in life support and/or safety applications is entirely at the buyer's risk, and the buyer agrees to defend, indemnify and hold harmless Microchip from any and all damages, claims, suits, or expenses resulting from such use. No licenses are conveyed, implicitly or otherwise, under any Microchip intellectual property rights.

Trademarks

The Microchip name and logo, the Microchip logo, dsPIC, KEELOQ, KEELOQ logo, MPLAB, PIC, PICmicro, PICSTART, PIC³² logo, rPIC and UNI/O are registered trademarks of Microchip Technology Incorporated in the U.S.A. and other countries.

FilterLab, Hampshire, HI-TECH C, Linear Active Thermistor, MXDEV, MXLAB, SEEVAL and The Embedded Control Solutions Company are registered trademarks of Microchip Technology Incorporated in the U.S.A.

Analog-for-the-Digital Age, Application Maestro, chipKIT, chipKIT logo, CodeGuard, dsPICDEM, dsPICDEM.net, dsPICworks, dsSPEAK, ECAN, ECONOMONITOR, FanSense, HI-TIDE, In-Circuit Serial Programming, ICSP, Mindi, MiWi, MPASM, MPLAB Certified logo, MPLIB, MPLINK, mTouch, Omniscient Code Generation, PICC, PICC-18, PICDEM, PICDEM.net, PICKit, PICtail, REAL ICE, rLAB, Select Mode, Total Endurance, TSHARC, UniWinDriver, WiperLock and ZENA are trademarks of Microchip Technology Incorporated in the U.S.A. and other countries.

SQTP is a service mark of Microchip Technology Incorporated in the U.S.A.

All other trademarks mentioned herein are property of their respective companies.

© 2002-2012, Microchip Technology Incorporated, Printed in the U.S.A., All Rights Reserved.

 Printed on recycled paper.

ISBN: 978-1-62076-089-5

**QUALITY MANAGEMENT SYSTEM
CERTIFIED BY DNV
= ISO/TS 16949 =**

Microchip received ISO/TS-16949:2009 certification for its worldwide headquarters, design and wafer fabrication facilities in Chandler and Tempe, Arizona; Gresham, Oregon and design centers in California and India. The Company's quality system processes and procedures are for its PIC[®] MCUs and dsPIC[®] DSCs, KEELOQ[®] code hopping devices, Serial EEPROMs, microperipherals, nonvolatile memory and analog products. In addition, Microchip's quality system for the design and manufacture of development systems is ISO 9001:2000 certified.



MICROCHIP

Worldwide Sales and Service

AMERICAS

Corporate Office
2355 West Chandler Blvd.
Chandler, AZ 85224-6199
Tel: 480-792-7200
Fax: 480-792-7277
Technical Support:
<http://www.microchip.com/support>
Web Address:
www.microchip.com

Atlanta
Duluth, GA
Tel: 678-957-9614
Fax: 678-957-1455

Boston
Westborough, MA
Tel: 774-760-0087
Fax: 774-760-0088

Chicago
Itasca, IL
Tel: 630-285-0071
Fax: 630-285-0075

Cleveland
Independence, OH
Tel: 216-447-0464
Fax: 216-447-0643

Dallas
Addison, TX
Tel: 972-818-7423
Fax: 972-818-2924

Detroit
Farmington Hills, MI
Tel: 248-538-2250
Fax: 248-538-2260

Indianapolis
Noblesville, IN
Tel: 317-773-8323
Fax: 317-773-5453

Los Angeles
Mission Viejo, CA
Tel: 949-462-9523
Fax: 949-462-9608

Santa Clara
Santa Clara, CA
Tel: 408-961-6444
Fax: 408-961-6445

Toronto
Mississauga, Ontario,
Canada
Tel: 905-673-0699
Fax: 905-673-6509

ASIA/PACIFIC

Asia Pacific Office
Suites 3707-14, 37th Floor
Tower 6, The Gateway
Harbour City, Kowloon
Hong Kong
Tel: 852-2401-1200
Fax: 852-2401-3431

Australia - Sydney
Tel: 61-2-9868-6733
Fax: 61-2-9868-6755

China - Beijing
Tel: 86-10-8569-7000
Fax: 86-10-8528-2104

China - Chengdu
Tel: 86-28-8665-5511
Fax: 86-28-8665-7889

China - Chongqing
Tel: 86-23-8980-9588
Fax: 86-23-8980-9500

China - Hangzhou
Tel: 86-571-2819-3187
Fax: 86-571-2819-3189

China - Hong Kong SAR
Tel: 852-2401-1200
Fax: 852-2401-3431

China - Nanjing
Tel: 86-25-8473-2460
Fax: 86-25-8473-2470

China - Qingdao
Tel: 86-532-8502-7355
Fax: 86-532-8502-7205

China - Shanghai
Tel: 86-21-5407-5533
Fax: 86-21-5407-5066

China - Shenyang
Tel: 86-24-2334-2829
Fax: 86-24-2334-2393

China - Shenzhen
Tel: 86-755-8203-2660
Fax: 86-755-8203-1760

China - Wuhan
Tel: 86-27-5980-5300
Fax: 86-27-5980-5118

China - Xian
Tel: 86-29-8833-7252
Fax: 86-29-8833-7256

China - Xiamen
Tel: 86-592-2388138
Fax: 86-592-2388130

China - Zhuhai
Tel: 86-756-3210040
Fax: 86-756-3210049

ASIA/PACIFIC

India - Bangalore
Tel: 91-80-3090-4444
Fax: 91-80-3090-4123

India - New Delhi
Tel: 91-11-4160-8631
Fax: 91-11-4160-8632

India - Pune
Tel: 91-20-2566-1512
Fax: 91-20-2566-1513

Japan - Osaka
Tel: 81-66-152-7160
Fax: 81-66-152-9310

Japan - Yokohama
Tel: 81-45-471-6166
Fax: 81-45-471-6122

Korea - Daegu
Tel: 82-53-744-4301
Fax: 82-53-744-4302

Korea - Seoul
Tel: 82-2-554-7200
Fax: 82-2-558-5932 or
82-2-558-5934

Malaysia - Kuala Lumpur
Tel: 60-3-6201-9857
Fax: 60-3-6201-9859

Malaysia - Penang
Tel: 60-4-227-8870
Fax: 60-4-227-4068

Philippines - Manila
Tel: 63-2-634-9065
Fax: 63-2-634-9069

Singapore
Tel: 65-6334-8870
Fax: 65-6334-8850

Taiwan - Hsin Chu
Tel: 886-3-5778-366
Fax: 886-3-5770-955

Taiwan - Kaohsiung
Tel: 886-7-536-4818
Fax: 886-7-330-9305

Taiwan - Taipei
Tel: 886-2-2500-6610
Fax: 886-2-2508-0102

Thailand - Bangkok
Tel: 66-2-694-1351
Fax: 66-2-694-1350

EUROPE

Austria - Wels
Tel: 43-7242-2244-39
Fax: 43-7242-2244-393

Denmark - Copenhagen
Tel: 45-4450-2828
Fax: 45-4485-2829

France - Paris
Tel: 33-1-69-53-63-20
Fax: 33-1-69-30-90-79

Germany - Munich
Tel: 49-89-627-144-0
Fax: 49-89-627-144-44

Italy - Milan
Tel: 39-0331-742611
Fax: 39-0331-466781

Netherlands - Drunen
Tel: 31-416-690399
Fax: 31-416-690340

Spain - Madrid
Tel: 34-91-708-08-90
Fax: 34-91-708-08-91

UK - Wokingham
Tel: 44-118-921-5869
Fax: 44-118-921-5820

11/29/11

Mouser Electronics

Authorized Distributor

Click to View Pricing, Inventory, Delivery & Lifecycle Information:

[Microchip:](#)

[TC7660COA713](#) [TC7660EPA](#) [TC7660IJA](#) [TC7660COA](#) [TC7660EOA713](#) [TC7660EOA](#) [TC7660MJA](#) [TC7660CPA](#)